Joseph Sweeney

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Research Focus

Digital ASIC design, high performance computing, obfuscation and security for digital ICs

Education

Carnegie Mellon University Pittsburgh, PA

PhD, MS Electrical and Computer Engineering - GPA: 3.73 *2021, 2017*

- Awards: Carnegie Institute of Technology Dean's Fellow, NSF Graduate Fellowship Honorable Mention
- Coursework Included: Advanced Digital IC Design, Machine Learning, Computer Architecture, Reconfigurable Logic, Numerical Methods and Optimization, Circuit Simulation, Digital System Testing

Columbia University New York, NY

BS Electrical and Computer Engineering - GPA: 3.9 *2015*

- Awards: Magna Cum Laude, Dean's List, Columbia Senior Design Project Award
- Coursework Included: Digital VLSI Circuits, Advanced Programming, Computer Networks, Data Structures, Computer Hardware Design, Solid State Devices, Device Microfabrication, Nanotechnology

Experience

Project Scientist/Graduate Researcher 2015 – Present

Center for Silicon System Implementation, Carnegie Mellon University *Pittsburgh, PA*

- Developed low-overhead circuit obfuscation methods that hide design function through programmable elements.
- Lead multiple successful accelerator tape-outs in 28/22/16nm technology nodes conducting system design, RTL implementation, synthesis, PNR, formal verification, and IC testing.
- Built and maintained research group's synthesis, physical design, and verification flows.
- Supervised PhD students/interns and lead weekly hardware security meetings.

Teaching Instructor 2018 – 2020

Department of Electrical and Computer Engineering, Carnegie Mellon University *Pittsburgh, PA*

- **Advanced Digital Integrated Circuit Design**: Established EDA flows and guided students in tape-out projects from development through IC testing.
- **Reconfigurable Logic**: Led recitations, developed labs in Vivado HLS/C++, and assisted students in class projects developing applications for FPGAs.
- **Introduction to Electrical and Computer Engineering**: Led recitations and wrote quizes to assess class understanding of lecture material.

VLSI/ASIC Engineering Intern 2014

Enterprise Servers Division, Hewlett Packard *Dallas, TX*

- Created online scheduling system to automate stability testing for in-development ASICs.
- Produced and maintained Tcl/Bash EDA scripts.

Selected Projects

Sparse Matrix-Vector Multiplication Accelerator | *Python, SystemVerilog, Genus, Innovus*

- Taped out accelerator for a novel sparse matrix-vector multiplication algorithm, co-optimizing between algorithm and underlying hardware.
- Designed micro-architecture utilizing custom synthesizable memory blocks for fine grained data access and multiple clock domains for power conservation.
- Using SystemVerilog and Innovus, iteratively optimized the design parameters and floorplan.
- Showed more than an order of magnitude improvement over current custom hardware solutions and more than two orders of magnitude improvement over commercial off-the-shelf architectures for both performance and energy efficiency.

Latch-Based Logic Locking | *Genus, Innovus, Japser Gold, SystemVerilog, Tcl, Tessent*

- Created a circuit obfuscation method that manipulates the clock phase of sequential elements, hiding functionality with negligible delay overhead.
- Developed a locking EDA flow compatible with standard industrial tools and verified the technique on common benchmark circuits through multiple tape-outs in 16/22nm nodes.
- Extended existing attack methods to account for the technique and demonstrated exponentially increasing attack times with minimal PPA overhead.

Analysis of Locked Circuits | *SAT, Python, Jasper Gold, Tessent, Genus*

- Created attack techniques for reverse-engineering obfuscation schemes using formal methods such as SAT, ATPG, and model checking.
- Established logic modeling techniques that enable key extraction in seconds for circuits that were previously unbreakable within weeks of run time.
- Demonstrated how Boolean sensitivity analysis can be used to deobfuscate circuits locked with a class of "provably secure" logic locking techniques.
- Updated broken obfuscation techniques with solutions for resisting the novel attack methods.

Technical Skills

Languages: Python, Tcl, C/C++
HDL: SystemVerilog, Verilog, Chisel, FIRRTL
Tools: Cadence Genus/Innovus/JasperGold/Virtuoso, Calibre DRC/LVS/PEX, Mentor Tessent, Xilinx Vivado
Software: Built and help maintain circuitgraph, a Python library for the manipulation of Boolean circuits.

Selected Publications

- P. Mohan, O. Atli, **J. Sweeney**, O. Kibar, L. Pileggi, and K. Mai, "Hardware Redaction via Designer-Directed Fine-Grained Soft eFPGA Insertion," Design, Automation and Test in Europe (DATE-21), February 2021.
- **J. Sweeney**, M. V. Zackriya, S. Pagliarini, and L. Pileggi, "Latch-Based Logic Locking," International Symposium on Hardware Oriented Security and Trust (HOST), December 2020. - ***Best Paper Nominee***
- **J. Sweeney**, M. J. H. Heule, and L. Pileggi, "Modeling Techniques for Logic Locking," International Conference on Computer Aided Design (ICCAD-39), November 2020.
- **J. Sweeney**, M. J. H. Heule, and L. Pileggi, "Sensitivity Analysis of Locked Circuits," International Conference on Logic for Programming, Artificial Intelligence and Reasoning (LPAR-23), May 2020.
- F. Sadi, **J. Sweeney**, T. M. Low, J. C. Hoe, L. Pileggi, and F. Franchetti, "Efficient SpMV Operation for Large and Highly Sparse Matrices using Scalable Multi-way Merge Parallelization," International Symposium on Microarchitecture (MICRO '52), October 2019.
- F. Sadi, **J. Sweeney**, S. McMillan, T. M. Low, J. Hoe, L. Pileggi, F. Franchetti, "PageRank Acceleration for Large Graphs with Scalable Hardware and Two-Step SpMV", IEEE HPEC Graph Challenge, September, 2018 - ***Student Innovation Award***

Co-Curricular

CMU ECE Graduate Organization
The CUT Magazine Writing Staff
Tau Beta Pi Engineering Honors Society
Columbia University Club Hockey